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PATENT APPLICATION

fee OK

2-12-03

L. Spruell

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Hiroataka KAWATA

Group Art Unit: 2815

Application No.: 09/617,441

Examiner: P. E. Brock II

Filed: July 14, 2000

Docket No.: 106310

For: ELECTRO-OPTICAL DEVICE AND ELECTRONIC
EQUIPMENT USING THE SAME

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AMENDMENT

Director of the U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

In reply to the November 1, 2002 Office Action, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Page 10, lines 8-20, delete current paragraph and insert therefor:

Fig. 3 is an expanded plan view of the TFT shown in Fig. 2. In Fig. 3, the gate-length direction is a direction in which the data line 6a extends, and the gate-width direction is a direction perpendicular to the gate-length direction. Each semiconductor layer 1a is electrically separated completely from the other semiconductor layers by a mesa-etching method, LOCOS method, or the like. The gate electrode 3 is provided on the semiconductor layer 1a through an insulating film. At least one portion of the ends in the gate-width direction of each gate electrode 3 is disposed on the semiconductor layer 1a, which does not extend toward the outside of the semiconductor layer 1a, as in a conventional TFT. The ends in the gate-length direction of the gate electrode 3 extend toward the outside of the channel